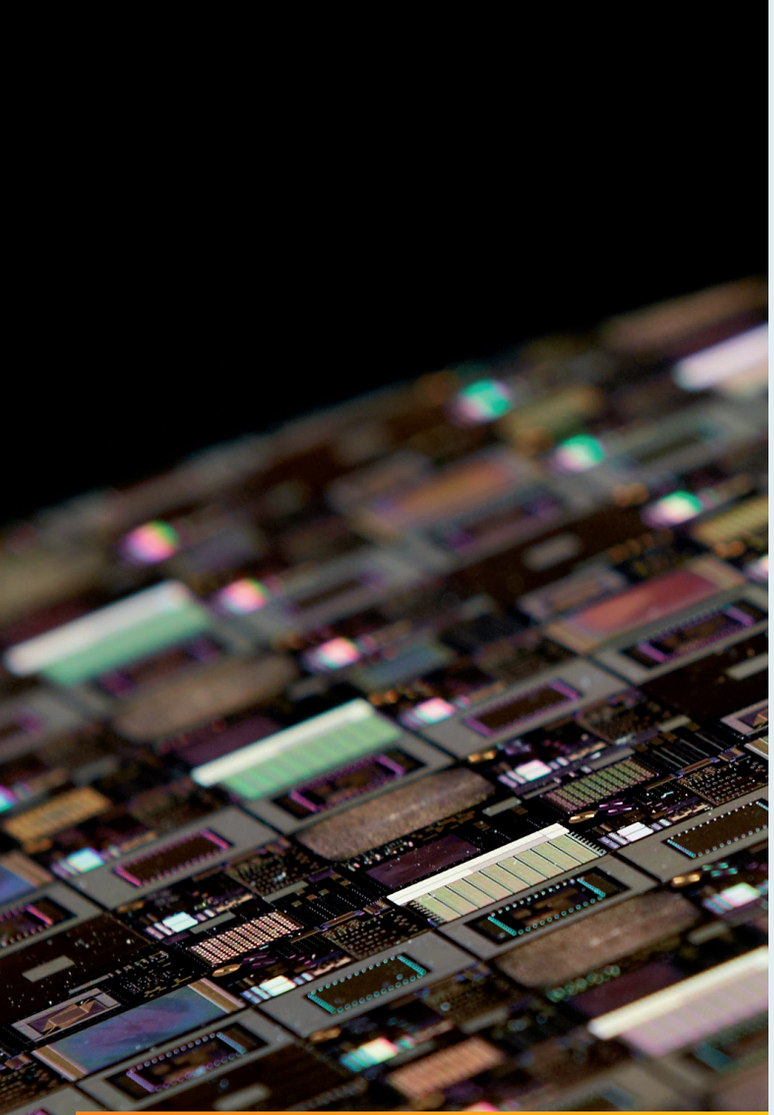

CEASAX – Strengthening Saxony as Europe's largest semiconductor location!«

Forschungsfabrik Mikroelektronik Deutschland

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SACHSEN

Contact

Dr. Manuela Junghähnel
Head of »All Silicon System Integration Dresden – ASSID«
Head of Department WLSI
at Fraunhofer IZM
Phone: +49 351 795572-18
manuela.junghaehnel@assid.izm.fraunhofer.de

Fraunhofer IZM
Ringstrasse 12
01468 Moritzburg
Germany

Dr. Wenke Weinreich
Deputy Institute Director and
Division Director »Center Nano-electronic Technologies« (CNT)
at Fraunhofer IPMS
Phone: +49 351 2607-3053
wenke.weinreich@ipms.fraunhofer.de

Fraunhofer IPMS
An der Bartlake 5
01109 Dresden
Germany

www.cmos-center.com

Fraunhofer

Center for Advanced CMOS and Heterointegration Saxony – CEASAX

Research Platform for 300 mm Frontend and Backend Wafer Level Integration

Combining 300 mm Frontend and Backend Technology

Platform for Active and Hetero-Integrated Systems

The Fraunhofer Center for Advanced CMOS & Heterointegration Saxony (CEASAX) bundles the competencies of the Fraunhofer Institute's IPMS-CNT and IZM-ASSID divisions for unique nationwide research with a broad process chain for microelectronic systems - from the front end to the back end on 300 mm.

As the appointed location for 300 mm wafer technologies in Saxony within the Fraunhofer clean room strategy, the center is part of the »Advanced Heterogenous System Integration Pilot Line« and a core of R&D value creation within the framework of the European Chips Act.

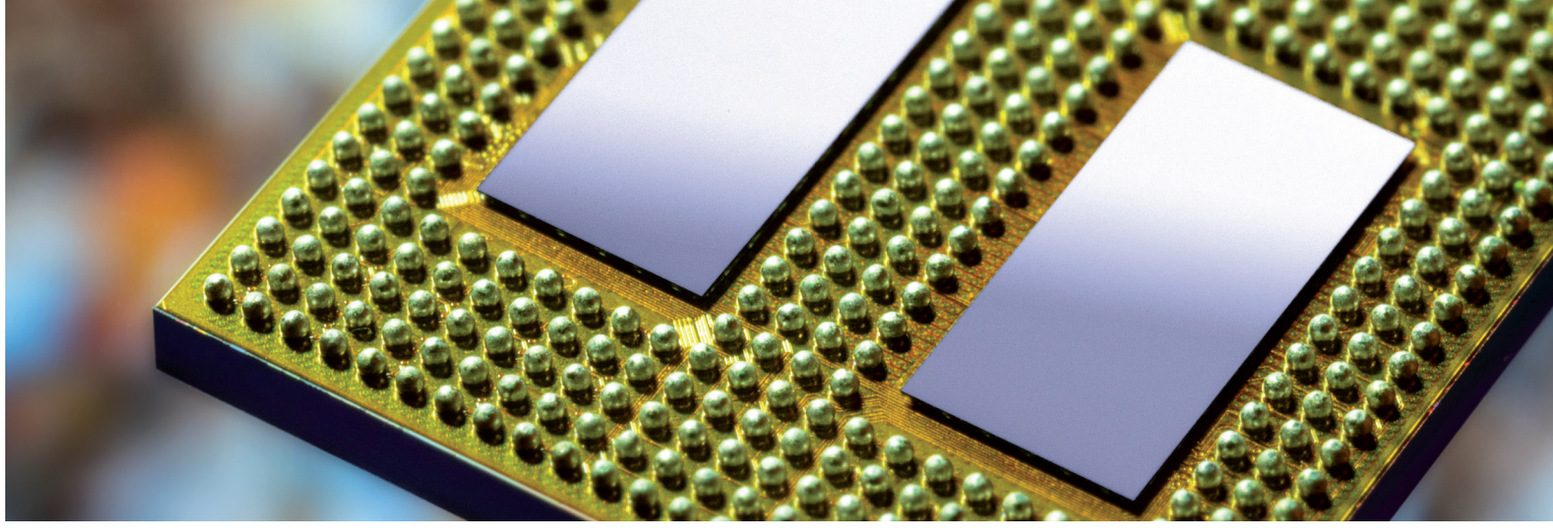
High Performance & Low Power Electronics

Technology Development for

- Chiplet Integration
- 3D Integration
- High density connections for nodes ≤ 10 nm

Application scenarios

- Neuromorphic computing
- Quantum computing
- Trusted Electronics
- Communication
- Si-Photonics



Portfolio for Industrial Applications

- Realization of intelligent sensor systems
- Future technologies for the development of chiplets
- Technology modules for HPC and AI
- Process solutions for wafer-level integration, 3D SiP and 3D wafer stacking
- Assembly and wafer-level packaging
- Advanced interposer technology for highly integrated SiPs

From Design to Front End to System on 300 mm

- Integrated passive/active components
- Emerging memories
- BEoL & FEoL CMOS technologies for ≤ 10 nm
- Post-FAB wafer processes
- High density 2.5D/3D wiring through active and passive interposers for high bandwidth and high frequency

Functionalized 300 mm Interposer Platform

The merging the scientific and technical competencies of the two key player enables an extended technology platform and value chain and thus the basis for the innovative integration of high-performance chips in major applications scenarios e.g. neuromorphic computing and trusted electronics.

CMOS Process and Device Development with Front End Integration

Heterogeneous Wafer-Level System Integration